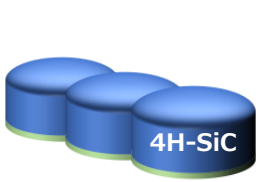
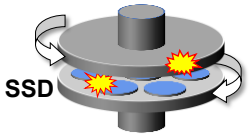
Advancing SiC Wafer Quality through Dynamic AGE-ing® and Multi-modal Signature Analysis

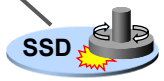
Company Overview: Core technologies

8" & Defects | *Material Loss* | *Quality variation from wafer to wafer* ⇄ *Suppress the defects* | *Bipolar degradation Switching loss*

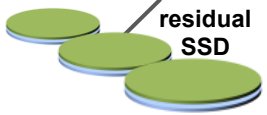








Cost vs. Quality



2500℃ **Crystal Growth** → **Slicing** ・Multi-wire saw ・Laser splitting → **Lapping/ Grinding** → **Mech.polish/ CMP** → 1650℃ **Epitaxy** → **MOSFET**

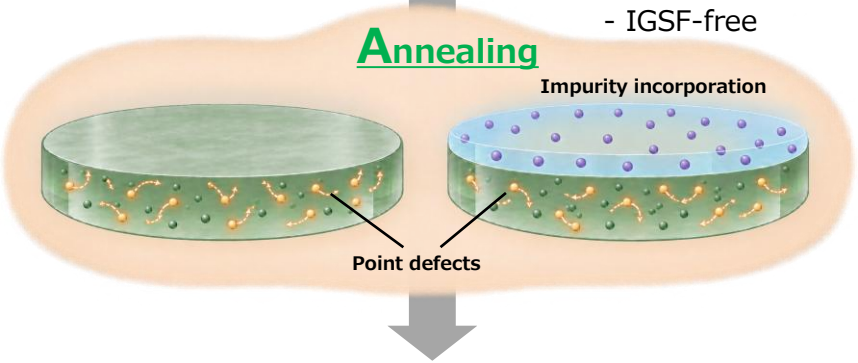
Dynamic AGE-ing®

Point-Defects engineering by Dynamic AGE-ing

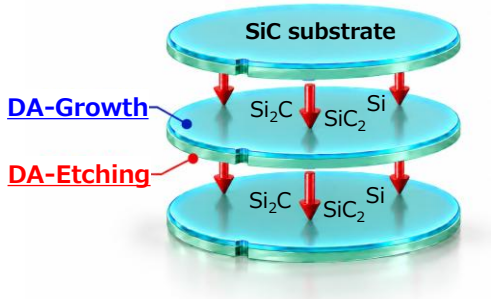
Thermal Etching (1600-2200℃) **Sublimation Growth**

- SSD-free
- BPD-free,
- IGSF-free

Annealing

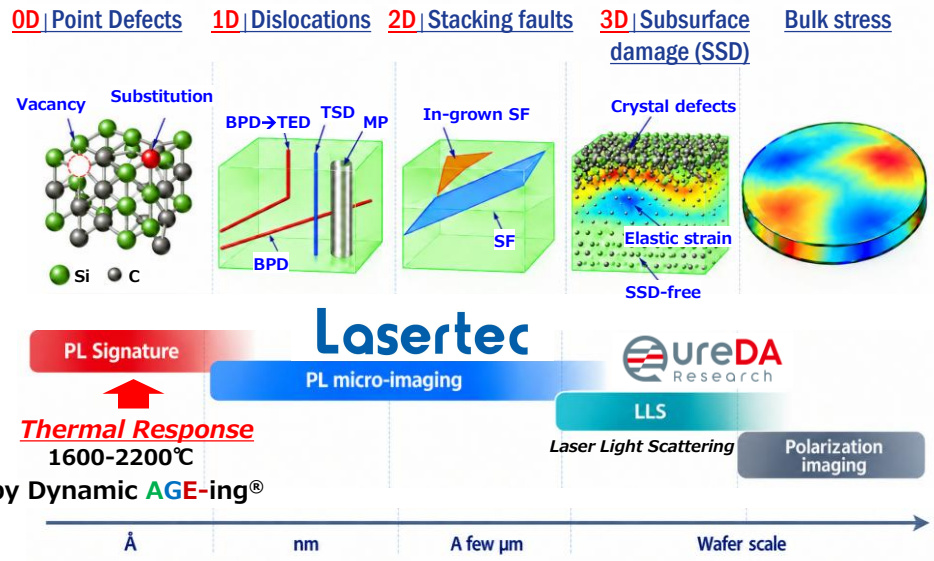


Point defect engineering ⇒ Carrier Lifetime Control

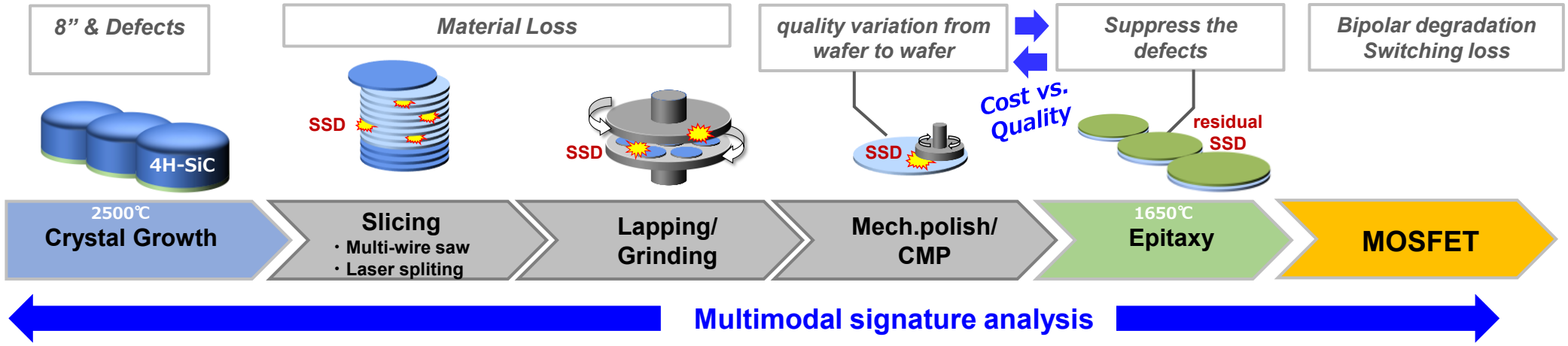


Noncontact-type manufacturing solution

Multimodal Signature analysis

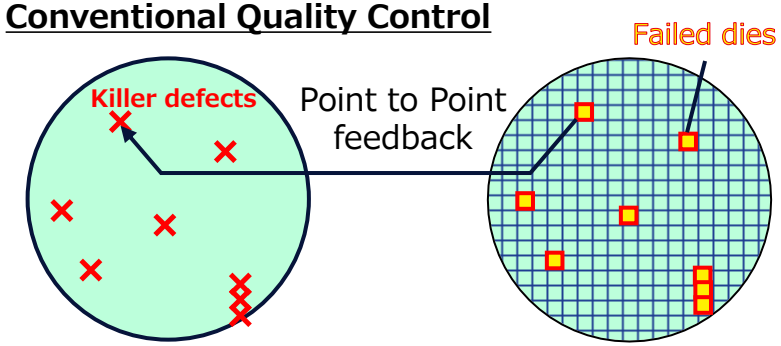


Advancing SiC Quality Control through Multimodal Signature Analysis

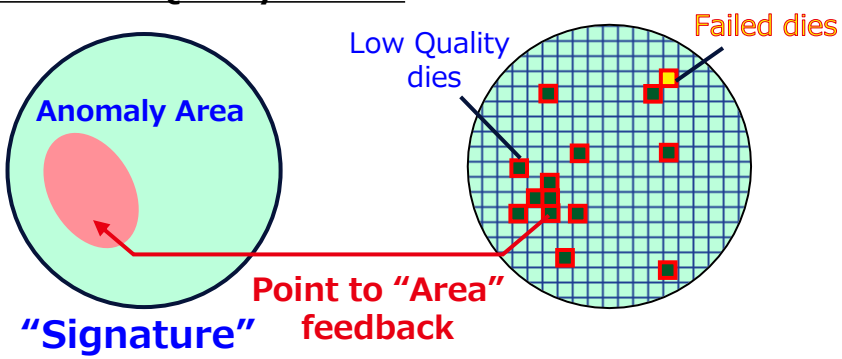


Multimodal signature analysis

■ **Conventional Quality Control**



■ **Advanced Quality control**



From Wafer Populations to Physical Mechanisms through Multimodal Signature Analysis

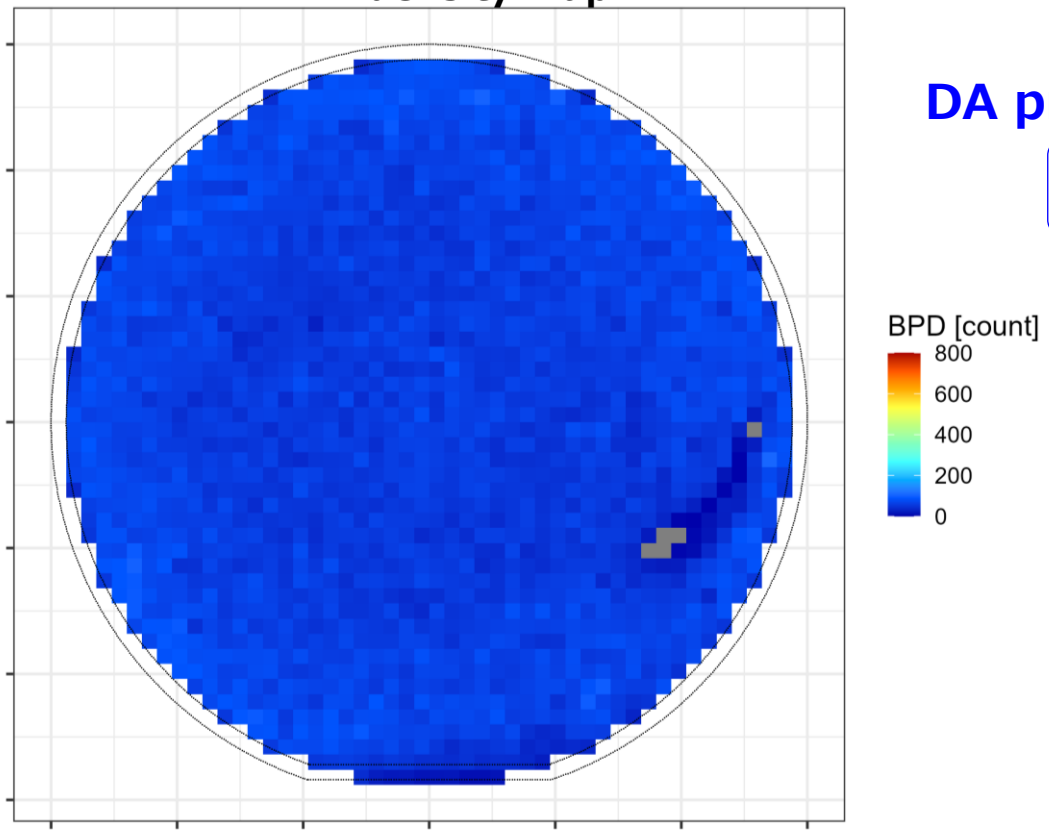
- ✓ **Is this defect typical or exceptional?**
- ✓ **Which process conditions promote or suppress defects?**
- ✓ **Can process responses help reveal physical mechanisms?**
  - ➢ Map **quality variations** across many wafers.
  - ➢ Use **process signatures** and controlled experiments to narrow possible causes.
  - ➢ Test whether proposed mechanisms explain population-wide quality variations.

Accelerate physical understanding and achieve reproducible quality improvements.

6-inch wafer Low-density BPD by DA process

■ BPD reduction in commercially available SiC wafers by a sequential process of “DA etching → growth”

Bare wafer
BPD density map

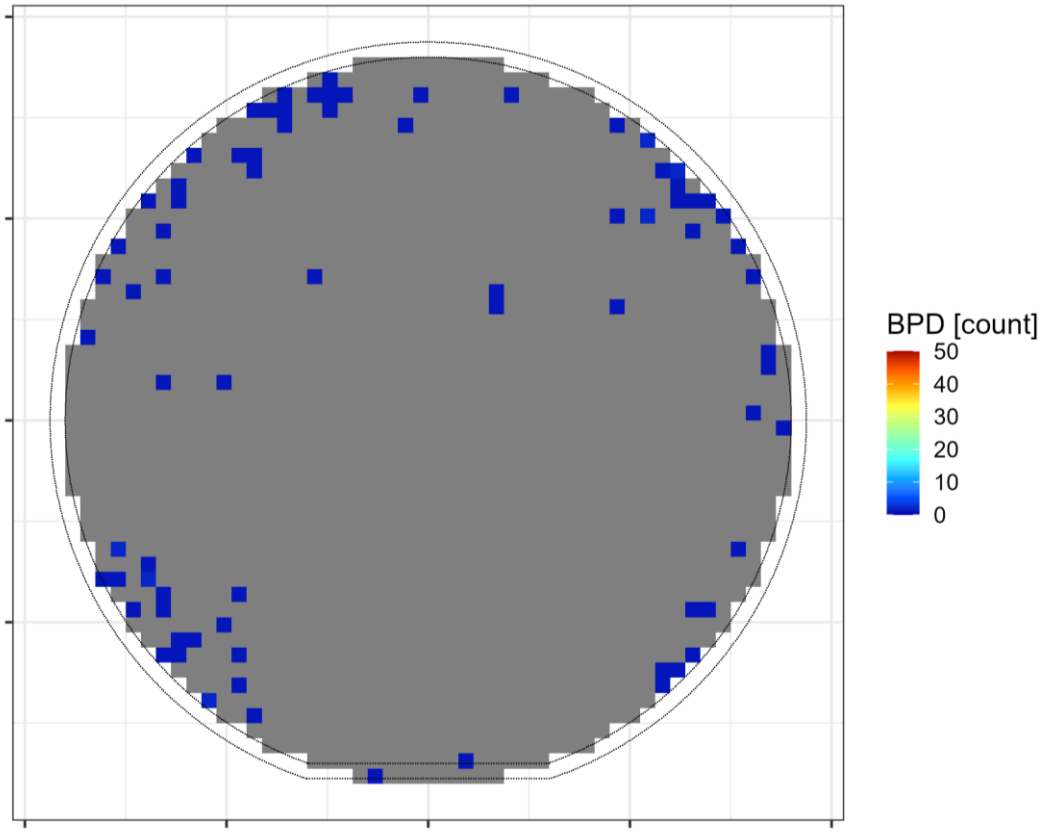


680 pieces/cm²

DA processing

DA etching
DA growth

Wafer after DA processing
BPD density map



0.5/cm2
BPD→TED conversion rate ≥99.9%

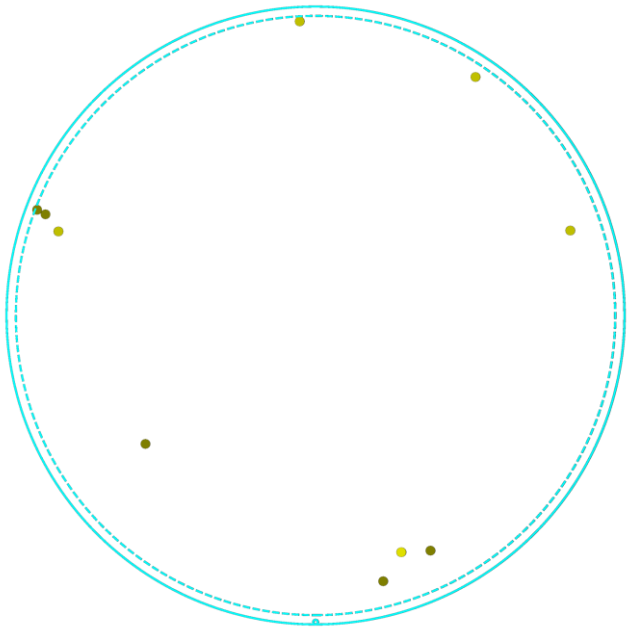
Stable high conversion rate from BPD to TED (≥99%)

8-inch wafer low-density in-grown stacking faults by DA process

■ **SF reduction in commercially available SiC wafers by a sequential process of “DA etching → growth”**

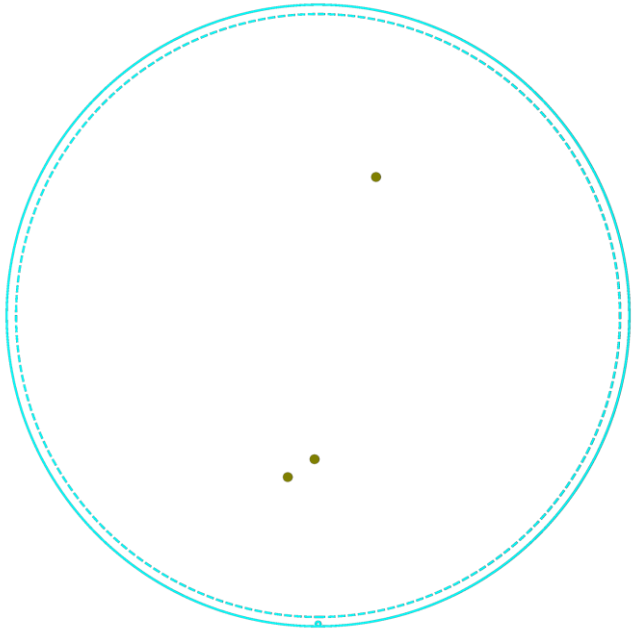
ICSCRM2026
Mo-P-18
(Posted at the K-3 booth)

Vendor



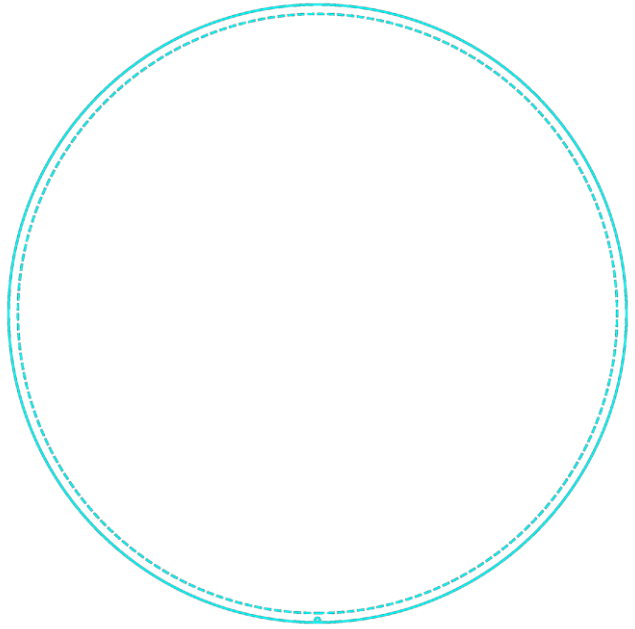
SF:0.05 /cm2

Vendor B



SF:0.04 /cm2

Vendor F



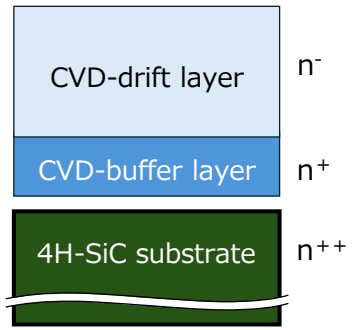
SF:0.00 /cm²

Improved DA processing and the reduction of SFs across multiple wafer manufacturers.

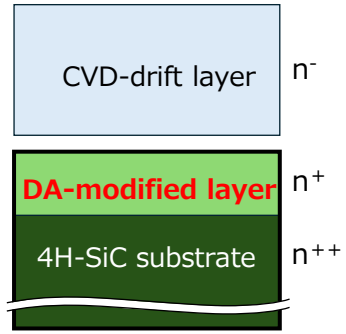
Substrate-integrated Point-defect Engineering by DA: Device Performance and Reliability

ICSCRM2026
Tu-P-99LN

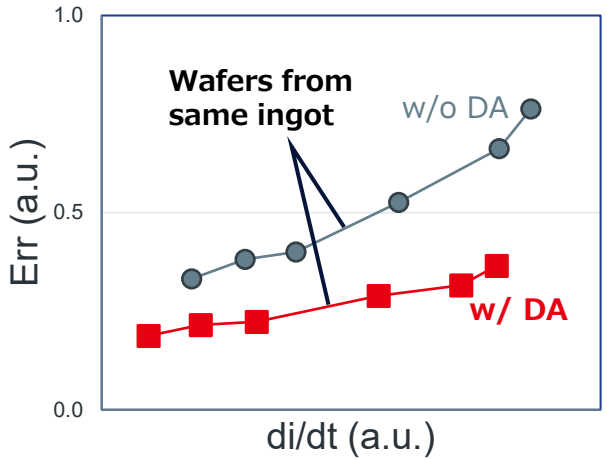
Reference
CVD-drift/buffer/ substrate



This study
CVD-drift layer / DA-modified substrate

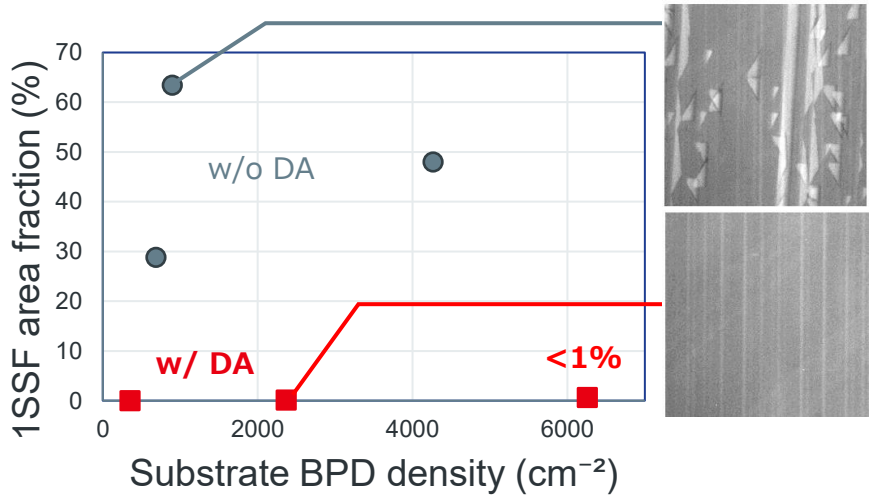


Lower reverse-recovery loss



Err: “40-50%” down

Suppressed bipolar degradation



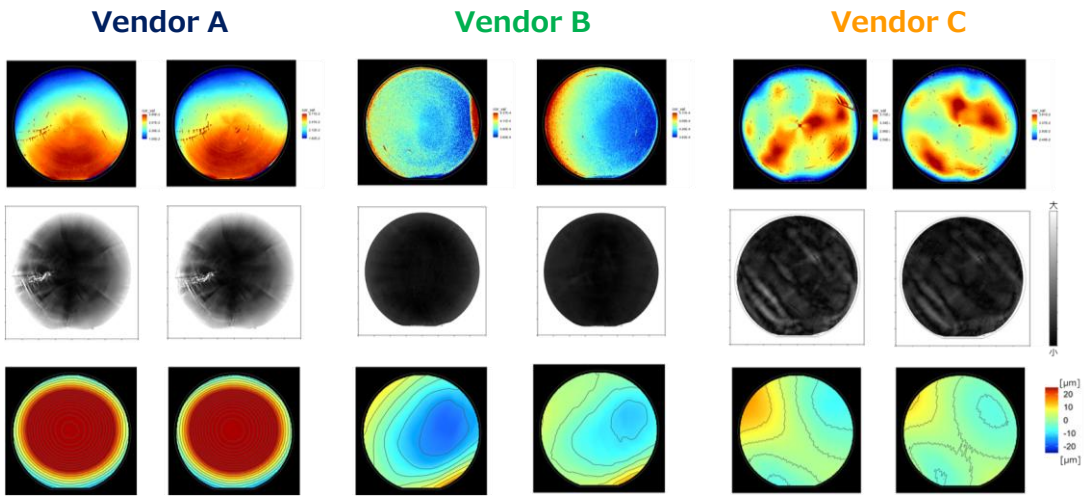
1SSF area: “<1%”

Applying DA enables device-optimized point-defect engineering

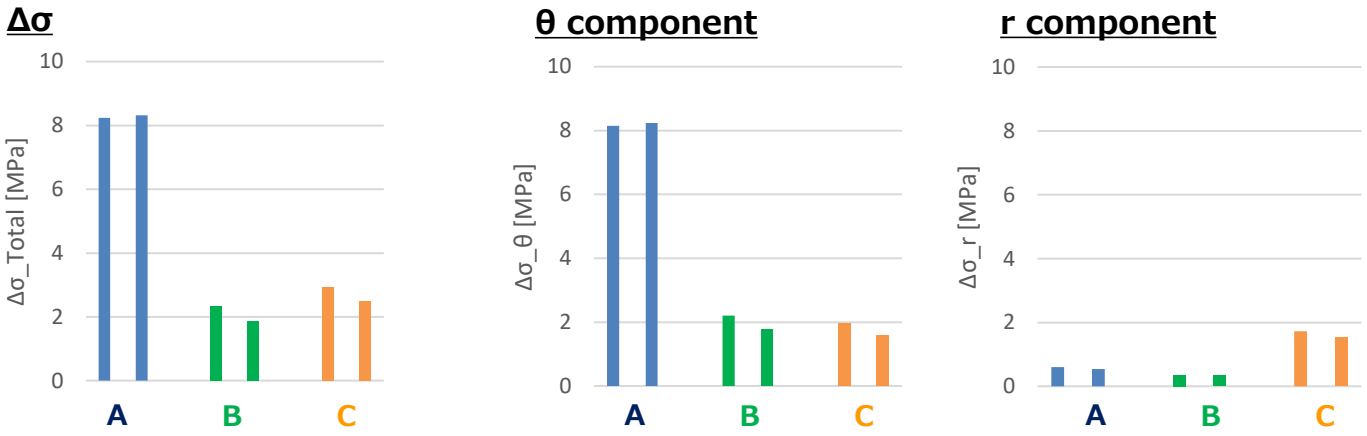
Advancing R&D toward mass production of the DA process

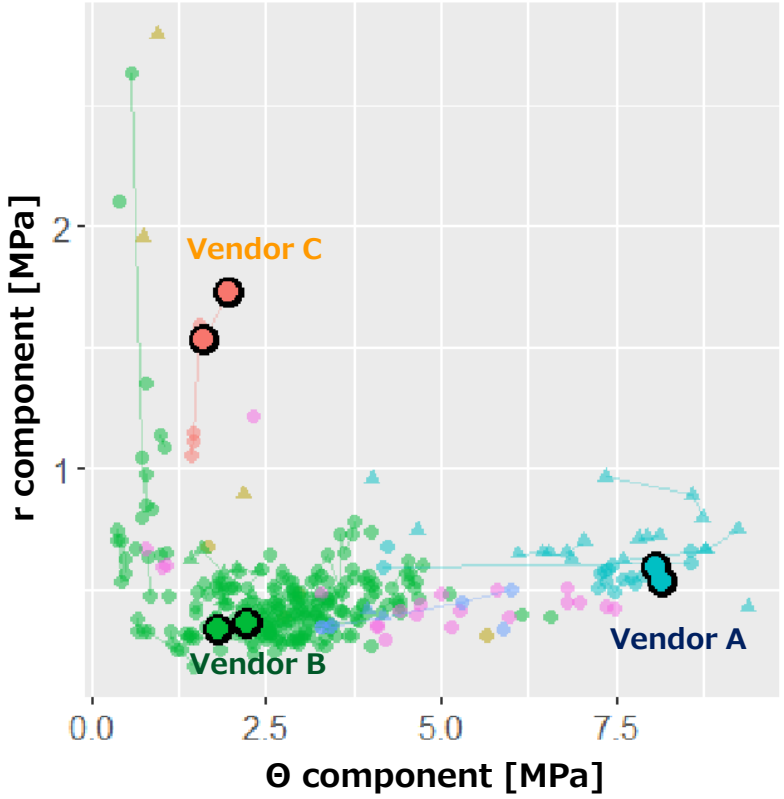
Target @ FY2027
>500 wafers/month
For both 6” and 8" inch

Proprietary classification technology



■ **Polarization imaging: Principal stress difference**





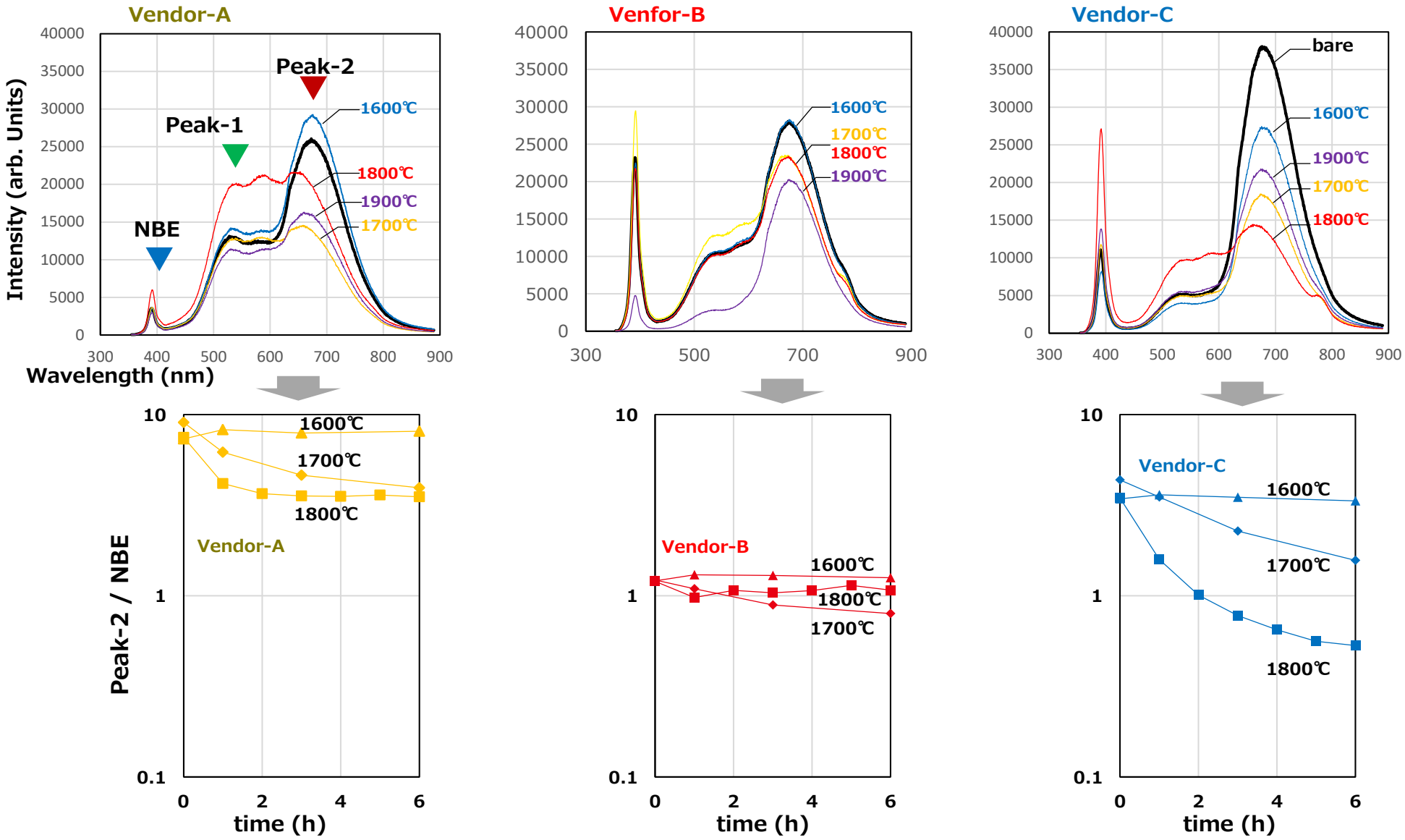
Classify wafers using proprietary analysis methods ➡ Various evaluations

Thermal-Response PL curve of 4H-SiC Wafers

ICSCRM2026
Tu-P-87LN

SiC wafers from different vendors

SiC wafer: as-purchased



Thermal response

1600-1800℃

by Dynamic AGE-ing®

Vendor-dependent thermal responses were observed in PL spectra following DA processing.

Lasertec-QureDA Collaborative Evaluation Platform



QureDA Research × Lasertec

Through Macro to Micro
Correlation to *"Causality"*

We-P-70	Toward Multiscale Evaluation of 4H-SiC Wafer Quality by Integrating Wafer-Scale Signatures and Microscopic Defect Inspection

QureDA Research Presentation list

Booth of QureDA Research, inc. : Exhibition-A, 1F, K-3

No.	Presentation Title
Mo-P-18	Defect Reduction in 8-inch 4H-SiC Wafers by Integrated Multi-Wafer Dynamic AGE-ing® Etching/Growth Process
We-P-70	Toward Multiscale Evaluation of 4H-SiC Wafer Quality by Integrating Wafer-Scale Signatures and Microscopic Defect Inspection
Th-P-70	Evaluation of the Effective C/Si Ratios during Thermal Etching and Growth on 4H-SiC(0001) Based on Macrostep Morphology
Tu-P-99LN	Substrate-Integrated Point-Defect Engineering by Dynamic AGE-ing for Suppressing Bipolar Degradation and Reverse-Recovery Loss in 4H-SiC MOSFETs
Tu-P-87LN	Thermal-Response PL/TR-PL Fingerprinting of B/Al-Dependent Lifetime Stability in n-Type 4H-SiC Wafers